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1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] Two or more 1st insulator layers embedded in two or more slots formed in the semi-conductor substrate, Two or more gate dielectric film formed on the above-mentioned semi-conductor substrate between the insulator layers of the above 1st, Two or more gate electrodes formed on two or more above-mentioned gate dielectric film, respectively, The impurity diffused layer formed into the above-mentioned semi-conductor substrate of two or more above-mentioned gate electrode both sides, The semiconductor device characterized by having the property that the transistors which are equipped with the 2nd insulator layer embedded two or more above-mentioned gate inter-electrode, and consist of the above-mentioned gate dielectric film, the above-mentioned gate electrode, and the above-mentioned impurity diffused layer differ for two or more fields of every.
[Claim 2] The transistor of a different property is a semiconductor device according to claim 1 characterized by having the thickness from which the thickness of gate dielectric film differs mutually, respectively.
[Claim 3] The transistor of a different property is a semiconductor device according to claim 1 or 2 characterized by consisting of the quality of the material from which the quality of the material of a gate electrode differs mutually, respectively.
[Claim 4] The semiconductor device according to claim 3 characterized by being the conductive film with which the quality of the material of a gate electrode contains a metal.
[Claim 5] In the manufacture approach of the semiconductor device which forms the transistor from which a property differs for two or more fields of every The 1st process which forms the mask film on a semi-conductor substrate, and the 2nd process which carries out patterning of the above-mentioned mask film and the above-mentioned semi-conductor substrate, and forms a slot, The 3rd process which embeds a separation insulator layer at above-mentioned Mizouchi, and the 4th process which removes the above-mentioned mask film of the field of the request of two or more above-mentioned fields, The 5th process which forms desired gate dielectric film on the above-mentioned semi-conductor substrate of the field of the above-mentioned request, The manufacture approach of the semiconductor device characterized by having with the 7th process which performs repeatedly the 6th process which forms the desired conductive film on the above-mentioned gate dielectric film, and the 4th process of the above, the 5th process and the 6th process to the field of other requests one by one.
[Claim 6] The 4th process of claim 5 is the manufacture approach of the semiconductor device characterized by performing a resist pattern as a mask.
[Claim 7] The 8th process which carries out patterning of the conductive film of the field of the request of two or more fields, and forms a gate electrode after the 7th process according to claim 5, The 9th process which forms an impurity diffused layer in the semi-conductor substrate of the both sides of the above-mentioned gate electrode, The manufacture approach of the semiconductor device characterized by having the process which performs repeatedly the 10th process which

embeds on the semi-conductor substrate between the both sides of the above-mentioned gate electrode, and a separation insulator layer, and forms an insulator layer, and the 8th process, the 9th process and the 10th process to the field of other requests one by one.
[Claim 8] In the manufacture approach of the semiconductor device which forms the transistor from which a property differs for two or more fields of every The 1st process which forms the mask film on a semi-conductor substrate, and the 2nd process which carries out patterning of the above-mentioned mask film and the above-mentioned semi-conductor substrate, and forms a slot, The 3rd process which embeds a separation insulator layer at above-mentioned Mizouchi, and the 4th process which carries out patterning of the above-mentioned mask film, and forms a dummy pattern, The 5th process which forms an impurity diffused layer in the above-mentioned semi-conductor substrate of the both sides of the above-mentioned dummy pattern, The 6th process which forms a pad insulator layer on the above-mentioned semi-conductor substrate between the both sides of the above-mentioned dummy pattern, and the above-mentioned separation insulator layer, The 8th process which removes the above-mentioned dummy pattern of the field of the request of two or more above-mentioned fields, The 9th process which forms desired gate dielectric film on the above-mentioned semi-conductor substrate of the above-mentioned dummy pattern removal field, The manufacture approach of the semiconductor device characterized by having the 11th process which performs repeatedly the 10th process which forms a desired gate electrode on the above-mentioned gate dielectric film, and the 8th process of the above, the 9th process and the 10th process to the field of a request of others [above] one by one.
[Claim 9] In the manufacture approach of the semiconductor device which forms the transistor from which a property differs for two or more fields of every The 1st process which carries out patterning of the semi-conductor substrate, and forms a slot, and the 2nd process which carries out flattening of the above-mentioned semi-conductor substrate front face by embedding a separation insulator layer at above-mentioned Mizouchi, The 3rd process which forms the 1st dummy film and the 2nd dummy film in the whole surface in order, The 4th process which carries out patterning of the dummy film of the above 2nd, and forms two or more dummy gate electrodes, The 5th process which forms an impurity diffused layer in the above-mentioned semi-conductor substrate of the both sides of two or more above-mentioned dummy gate electrodes, The 6th process which forms an insulator layer so that two or more above-mentioned dummy gate electrodes may be covered, The 7th process which carries out flattening until the above-mentioned dummy gate electrode exposes the above-mentioned insulator layer, The 8th process which removes the above-mentioned dummy gate electrode of the field of the request of two or more above-mentioned fields, and the 1st dummy film, The 9th process which forms desired gate dielectric film on the above-mentioned semi-conductor substrate of the above-mentioned dummy gate electrotreatment field, The manufacture approach of the semiconductor device characterized by having the 11th process which performs repeatedly the 10th process which forms a desired gate electrode on the above-mentioned gate dielectric film, and the 8th process of the above, the 9th process and the 10th process to the field of a request of others [above] one by one.
[Claim 10] The thickness of gate dielectric film is the manufacture approach of the semiconductor device according to claim 5 to 9 characterized by forming in different thickness for every field.
[Claim 11] The ingredient of a gate electrode is the manufacture approach of the semiconductor device according to claim 5 to 10 characterized by forming with a different ingredient for every field.

[Claim 12] The manufacture approach of the semiconductor device according to claim 7 to 9 characterized by having the process which forms a wiring layer on a gate electrode.
[Claim 13] The process which forms a wiring layer on a gate electrode is the manufacture approach of the semiconductor device according to claim 12 characterized by being the process which removes the above-mentioned gate electrode, the process which forms the conductive film in the whole surface, and the process which carries out patterning of the above-mentioned conductive

film, and unifies and forms the above-mentioned wiring layer and the above-mentioned gate electrode.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention relates to the manufacture approach of a semiconductor device of having MISFET structure, about the manufacture approach of a semiconductor device.
[0002]
[Description of the Prior Art] It has come to form the component which has a different function in the same semiconductor chip as high integration of a semiconductor device and advanced features progress. For this reason, it is necessary to form the transistor which has a different operating characteristic, i.e., the transistor which has a different threshold, in the same LSI. Then, the transistor from which the thickness of gate dielectric film differs is formed in the same LSI as a transistor which has a different threshold.
[0003] Drawing 13 and 14 are the process sectional views showing the manufacture approach of the conventional semiconductor device. Sequential explanation is given according to drawing. First, as shown in drawing 13 (a), 10nm of silicon oxide is formed as 1st mask film 102 with the oxidizing [thermally] method or a CVD method on the semi-conductor substrate 101. Next, 150nm for example, of silicon nitrides is formed as 2nd mask film 103 with a CVD method. Then, a desired resist pattern (with no illustration) is formed by photoengraving process, and a trench 104 is formed in the semi-conductor substrate 101 by the etching method.
[0004] Next, as shown in drawing 13 (b), after forming silicon oxide in the whole surface as the 1st insulator layer 105 with a CVD method, the 1st insulator layer 105 on the 2nd mask film 103 is removed carrying out flattening by the grinding method, and the 1st insulator layer 105 is embedded in a trench 104.
[0005] Next, as shown in drawing 13 (c), after reducing the thickness of the 1st insulator layer 105 in a trench 104 by the wet etching methods, such as fluoric acid, the 2nd mask film 103 is alternatively removed by the wet etching methods, such as a heat phosphoric acid. Then, the 1st mask film 102 is further removed by the wet etching method.
[0006] Next, as shown in drawing 13 (d), about 2nm of silicon oxide is formed as 1st thermal oxidation film 106 by the oxidizing [thermally] method. Next, as shown in drawing 14 (a), the resist film 107 is formed in a predetermined field with a photo-engraving process, and the 1st thermal oxidation film 106 which is not covered with the resist film 107 is removed by wet etching or the dry etching method.

[0007] Next, as shown in drawing 14 (b), after removing the resist film 107 by the ashing method etc., 2nm of silicon oxide is formed as 2nd thermal oxidation film 108 by the oxidizing [thermally] method. Consequently, in the field which remains without removing the 1st thermal oxidation film 106, the 2nd thermal oxidation film 108 will be formed on the 1st thermal oxidation film 106, and the thickness of the thermal oxidation film increases. Thereby, the field which has the thermal oxidation film with which thickness differs is formed in the same LSI.
[0008] Next, as shown in drawing 14 (c), after forming 200nm of conductive film, such as polish recon and an amorphous silicon, for example, the gate electrodes 109a and 109b and gate dielectric film 110 and 111 are formed by photoengraving process and the etching method.
[0009] At this time, the 1st gate dielectric film 110 which becomes the lower part of gate electrode 109a from the 2nd thermal oxidation film 108 is formed, and the 2nd gate dielectric film 111 which consists of the 1st thermal oxidation film 106 and the 2nd thermal oxidation film 108 is formed in the lower part of gate electrode 109b. The thickness of the 2nd gate dielectric film 111 is thicker than the thickness of the 1st gate dielectric film 110 with a natural thing, and it is formed.
[0010] Then, P, As, or B and BF2 are poured in by injection rate 1E13-1E14/cm2 with ion-implantation, and the 1st impurity diffused layer 112 is formed. Furthermore, after forming silicon oxide or 50-100nm of silicon nitrides etc. with a CVD method, a sidewall 113 is formed by the etching method. Then, P, As, or B and BF2 are poured in by injection rate 1E15-1E16/cm2 with ion-implantation, and the 2nd impurity diffused layer 114 is formed. Thus, the transistor from which the thickness of the 1st gate dielectric film 110 and the thickness of the 2nd gate dielectric film 111 differ is formed.
[0011]
[Problem(s) to be Solved by the Invention] The manufacture approach of the conventional semiconductor device is above, in order to form different gate dielectric film in the same LSI, two thermal oxidation is performed, and there was a trouble that one gate dielectric film would pass through the heat treatment process of 2 times, and tends to receive the fluctuation factor of a process at the time of formation of gate dielectric film.
[0012] Moreover, since the 2nd thermal oxidation film was formed in right above [of the 1st thermal oxidation film used as gate dielectric film] through the process of forming and removing the resist film, there was a trouble that ****** of the resist film which is not expected in the removal process of the resist film occurred. Furthermore, there was a trouble that the thermal oxidation film which turns into gate oxide by ****** of this resist film was polluted.
[0013] Moreover, although the above-mentioned Prior art does not explain, in order to remove ****** of the resist film, the washing process is performed after resist film removal. In this washing process, when the penetrant remover to be used was liquid with some etching operations, the 1st thermal oxidation film will be etched and there was a trouble that the thickness of a request of gate dielectric film was not obtained.
[0014] Furthermore, in case the 1st thermal oxidation film is removed, the 1st insulator layer in a trench is etched, it retreats into a trench, and the 1st insulator layer front face becomes low from a semi-conductor substrate front face. Consequently, a crevice will be formed in the trench upper part. When the transistor was formed after that, metal-oxide-semiconductor structure was formed in the side attachment wall of the crevice of the trench upper part, and there was a trouble of degrading the property of a transistor, by the so-called reverse narrow channel effect.
[0015] It aims at offering the manufacture approach of the semiconductor device which this invention can form respectively independently the gate electrode which was made in order to cancel the above troubles, and consists of the gate dielectric film and the different quality of the material of different thickness in the same LSI, and can form the transistor which has a different property with the yield sufficient good in the same LSI.
[0016]
[Means for Solving the Problem] Two or more 1st insulator layers embedded in two or more slots

where the semiconductor device concerning claim 1 of this invention was formed in the semi-conductor substrate, Two or more gate dielectric film formed on the above-mentioned semi-conductor substrate between the insulator layers of the above 1st, Two or more gate electrodes formed on two or more above-mentioned gate dielectric film, respectively, The impurity diffused layer formed into the above-mentioned semi-conductor substrate of two or more above-mentioned gate electrode both sides, It has the 2nd insulator layer embedded two or more above-mentioned gate inter-electrode, and is made to have the property that the transistors which consist of gate dielectric film, a gate electrode, and an impurity diffused layer differ for two or more fields of every.
[0017] It is made for the transistor which has the property that the semiconductor devices concerning claim 2 of this invention differ to have the thickness from which gate dielectric film differs mutually.
[0018] It is made for the transistor of the property that the semiconductor devices concerning claim 3 of this invention differ to consist of the quality of the material from which the quality of the material of a gate electrode differs, respectively mutually.
[0019] It is made for the semiconductor device concerning claim 4 of this invention to be conductive film with which the quality of the material of a gate electrode contains a metal.
[0020] The manufacture approach of the semiconductor device concerning claim 5 of this invention The 1st process which forms the mask film on a semi-conductor substrate, and the 2nd process which carries out patterning of the above-mentioned mask film and the above-mentioned semi-conductor substrate, and forms a slot, The 3rd process which embeds a separation insulator layer at above-mentioned Mizouchi, and the 4th process which removes the above-mentioned mask film of the field of the request of two or more above-mentioned fields, It has with the 7th process which performs repeatedly the 5th process which forms desired gate dielectric film on the above-mentioned semi-conductor substrate of the field of the above-mentioned request, the 6th process which forms the desired conductive film on the above-mentioned gate dielectric film, and the 4th process of the above, the 5th process and the 6th process to the field of other requests one by one.
[0021] The 4th process of claim 5 is made for the manufacture approach of the semiconductor device concerning claim 6 of this invention to perform a resist pattern as a mask.
[0022] The manufacture approach of the semiconductor device concerning claim 7 of this invention The 8th process which carries out patterning of the conductive film of the field of the request of two or more fields, and forms a gate electrode after the 7th process according to claim 5, The 9th process which forms an impurity diffused layer in the semi-conductor substrate of the both sides of the above-mentioned gate electrode, It has the process which performs repeatedly the 10th process which embeds on the semi-conductor substrate between the both sides of the above-mentioned gate electrode, and a separation insulator layer, and forms an insulator layer, and the 8th process, the 9th process and the 10th process to the field of other requests one by one.
[0023] The manufacture approach of the semiconductor device concerning claim 8 of this invention The 1st process which forms the mask film on a semi-conductor substrate, and the 2nd process which carries out patterning of the above-mentioned mask film and the above-mentioned semi-conductor substrate, and forms a slot, The 3rd process which embeds a separation insulator layer at above-mentioned Mizouchi, and the 4th process which carries out patterning of the above-mentioned mask film, and forms a dummy pattern, The 5th process which forms an impurity diffused layer in the above-mentioned semi-conductor substrate of the both sides of the above-mentioned dummy pattern, The 6th process which forms a pad insulator layer on the above-mentioned semi-conductor substrate between the both sides of the above-mentioned dummy pattern, and the above-mentioned separation insulator layer, The 8th process which removes the above-mentioned dummy pattern of the field of the request of two or more above-mentioned fields, The 9th process which forms desired gate dielectric film on the above-mentioned semi-conductor substrate of the above-mentioned dummy pattern removal field, It has the 11th process which performs repeatedly

the 10th process which forms a desired gate electrode on the above-mentioned gate dielectric film, and the 8th process of the above, the 9th process and the 10th process to the field of a request of others [above] one by one.

[0024] The manufacture approach of the semiconductor device concerning claim 9 of this invention The 1st process which carries out patterning of the semi-conductor substrate, and forms a slot, and the 2nd process which carries out flattening of the above-mentioned semi-conductor substrate front face by embedding an insulator layer at above-mentioned Mizouchi, The 3rd process which forms the 1st dummy film and the 2nd dummy film in the whole surface in order, The 4th process which carries out patterning of the dummy film of the above 2nd, and forms two or more dummy gate electrodes, The 5th process which forms an impurity diffused layer in the above-mentioned semi-conductor substrate of the both sides of two or more above-mentioned dummy gate electrodes, The 6th process which forms an insulator layer so that two or more above-mentioned dummy gate electrodes may be covered, The 7th process which carries out flattening until the above-mentioned dummy gate electrode exposes the above-mentioned insulator layer, The 8th process which removes the above-mentioned dummy gate electrode of the field of the request of two or more above-mentioned fields, and the 1st dummy film, The 9th process which forms desired gate dielectric film on the above-mentioned semi-conductor substrate of the above-mentioned dummy gate electrotreatment field, It has the 11th process which performs repeatedly the 10th process which forms a desired gate electrode on the above-mentioned gate dielectric film, and the 8th process of the above, the 9th process and the 10th process to the field of a request of others [above] one by one.

[0025] The manufacture approach of the semiconductor device concerning claim 10 of this invention forms the thickness of gate dielectric film in different thickness for every field.

[0026] The manufacture approach of the semiconductor device concerning claim 11 of this invention forms the ingredient of a gate electrode with a different ingredient for every field.

[0027] The manufacture approach of the semiconductor device concerning claim 12 of this invention is equipped with the process which forms a wiring layer on a gate electrode.

[0028] The processes at which the manufacture approach of the semiconductor device concerning claim 13 of this invention forms a wiring layer on a gate electrode are the process which removes the above-mentioned gate electrode, the process which forms the conductive film in the whole surface, and a process which carries out patterning of the above-mentioned conductive film, and unifies and forms the above-mentioned wiring layer and the above-mentioned gate electrode.

[0029]

[Embodiment of the Invention] Gestalt 1. drawing 1 of operation - drawing 4 are the process sectional views showing the manufacture approach of the semiconductor device of the gestalt 1 implementation this invention. Sequential explanation is given according to drawing.

[0030] First, as shown in drawing 1 (a), about 10-20nm of silicon oxide is formed as 1st mask film 2 with the oxidizing [thermally] method or a CVD method on the semi-conductor substrate 1. Next, polish recon or about 200-400nm of silicon nitrides are formed as 2nd mask film 3 with a CVD method. Then, a desired resist pattern (with no illustration) is formed by photoengraving process, and patterning of the 1st and 2nd mask film 2 and 3 is carried out. After removing a resist pattern, the trench 4 of the shape of a quirk which consists of the 1st and 2nd mask film 2 and 3 and semi-conductor substrates 1 by the etching method is formed by using as a mask the 1st and 2nd mask film 2 and 3 which carried out patterning so that the depth in the semi-conductor substrate 1 may change with about 20-50nm.

[0031] Next, as shown in drawing 1 (b), after forming about 100-500nm of silicon oxide in the whole surface as the 1st insulator layer 5 with a CVD method, the 1st insulator layer 5 on the 2nd mask film 3 is removed carrying out flattening by the grinding method or the etchback method, and the 1st insulator layer 5 as a separation insulator layer is embedded only in a trench 4.

[0032] Next, as shown in drawing 1 (c), a resist pattern 70 is formed so that it may cover except the

field of the request for forming the 1st gate dielectric film 10. At this time, a resist pattern 70 is formed on the 1st insulator layer 5 and the 2nd mask film 3. Next, the 2nd mask film 3 is removed by using a resist pattern 70 as a mask. Then, after removing the 1st mask film 2, it washes by removing a resist pattern 70 (drawing 1 (d)).

[0033] Next, as shown in drawing 2 (a), it forms by silicon oxide conversion as the 1st gate dielectric film 10 with the oxidizing [thermally] method or a CVD method at about 1-5nm. Next, as shown in drawing 2 (b), the cascade screen which consists of the polish recon film, the amorphous silicon film, the metal silicification film, a metal nitride, a metal membrane, or these two film or more as conductive film is formed, flattening is carried out to the whole surface by the grinding method or the etchback method, and the 1st conductive film 15 is formed in it.

[0034] Thus, if the 1st gate dielectric film 10 is formed, a resist pattern 70 will not contact the 1st gate dielectric film 10 directly. Therefore, in a resist removal process, resist ** is not generated on the 1st gate dielectric film 10. Moreover, in the washing process after a resist removal process, film decrease does not arise in the 1st gate dielectric film 10.

[0035] Next, as shown in drawing 2 (c), the 1st mask film 2 of the field for forming the 2nd gate dielectric film 11 and the 2nd mask film 3 are removed by performing photoengraving process and etching through the same process as drawing 1 (c) and (d).

[0036] Next, as shown in drawing 2 (d), silicon oxide, a silicon nitride, a metal oxide film, a metal nitriding oxide film, etc. are formed as the 2nd desired gate dielectric film 11 with the oxidizing [thermally] method or a CVD method through the same process as drawing 2 (a). At this time, the thickness of the 2nd gate dielectric film 11 is formed so that it may differ from the thickness of the 1st gate dielectric film 10, for example, it is formed by about 1-10nm by silicon oxide conversion.

[0037] Then, like drawing 2 (b), the polish recon film, the metal silicification film, a metal nitride, a metal membrane, or these two cascade screens or more are formed as conductive film, flattening is carried out to the whole surface by the grinding method or the etchback method, and the 2nd conductive film 16 is formed in it.

[0038] If it does in this way, the 1st gate dielectric film and 2nd gate dielectric film with which thickness differs can be separately formed independently. Therefore, heat treatment in the case of formation of the gate dielectric film of desired thickness or a membrane formation process can be performed by once, respectively, and minimum suppresses fluctuation of the gate dielectric film by process fluctuation.

[0039] Moreover, since each resist pattern does not contact gate dielectric film directly, resist ****** does not occur on gate dielectric film, and film decrease of each gate dielectric film does not arise in the washing process after a resist removal process.

[0040] Then, as shown in drawing 3 (a), a resist pattern 17 is formed with a photo-engraving process. Next, as shown in drawing 3 R> 3 (b), the 1st conductive film 15 is etched by using a resist pattern 17 as a mask, and 1st gate electrode 9a is formed.

[0041] Next, as shown in drawing 3 (c), P, As, or B and BF2 are poured in by injection rate 1E13-1E14/cm2 with ion-implantation, and 1st impurity diffused layer 12a is formed. Furthermore, after forming silicon oxide or 50nm of silicon nitrides etc. with a CVD method, 1st sidewall 13a is formed by the etchback method. Then, P, As, or B and BF2 are poured in by injection rate 1E15-1E16/cm2 with ion-implantation, and 2nd impurity diffused layer 14a is formed.

[0042] Next, as shown in drawing 3 (d), 500nm of silicon oxide etc. is formed with a CVD method etc., flattening is carried out by the grinding method or the etchback method, and the pad insulator layer 18 is formed on the semi-conductor substrate between the 1st insulator layer 5 of the both sides of 1st gate electrode 9a. Thus, a desired field is made to complete a desired transistor.

[0043] As shown in drawing 4 (a), after forming 2nd gate electrode 9b, the 3rd impurity diffused layer 12b, the 2nd sidewall 13b, and 4th impurity diffused layer 14b by repeating the same process as drawing 3 (a) - (d), the pad insulator layer 18 is formed. Thus, other fields are made to complete a desired transistor.

[0044] Next, as shown in drawing 4 (b), metal silicide, such as metal nitrides, such as metal membranes, such as aluminum, Cu, W, and Ta, and TiN, TaN, WN, and nickel, Co, Ti, W, Ta, and about 20nm of conductive film 19 which consists of polish recons, etc. these alloys, or a cascade screen further are formed in the whole surface by the CVD method or PVD. Next, as shown in drawing 4 (c), a wiring layer 20 is formed by giving photoengraving process and the etching method to the conductive film 19.

[0045] In two or more fields, since the semiconductor device of the gestalt 1 of the operation constituted as mentioned above can form a transistor in each field independently, it can form independently desired gate dielectric film and a desired gate electrode separately, and can form the transistor which has a different property good. Furthermore, the 1st insulator layer is projected and formed on the semi-conductor substrate, retreats from a semi-conductor substrate front face, and does not form a crevice. Therefore, metal-oxide-semiconductor structure is formed in the side attachment wall of a crevice, unnecessary electric field are generated, and it can prevent degrading the property of a transistor.

[0046] Although the case where an impurity diffused layer was formed was explained with the gestalt 1 of the gestalt 2. above-mentioned implementation of operation after forming a gate electrode and gate dielectric film, how to form a gate electrode and gate dielectric film is explained after forming an impurity diffused layer here.

[0047] Drawing 5 - drawing 7 are the process sectional views showing the manufacture approach of the semiconductor device of the gestalt 2 implementation this invention. Sequential explanation is given according to drawing. First, after forming the 1st mask film 2, the 2nd mask film 3, and a trench 4 on the semi-conductor substrate 1 through the same process as drawing 1 (a) of the gestalt 1 of the above-mentioned implementation, and (b), the 1st insulator layer 5 as a separation insulator layer is embedded in a trench 4.

[0048] Next, as shown in drawing 5 (a), the resist pattern 21 for dummy pattern formation is formed with a photo-engraving process. Next, as shown in drawing 5 (b), only the 2nd mask film 3 is etched and 1st dummy pattern 22a is formed.

[0049] Next, as shown in drawing 5 (c), an ion implantation is performed by using 1st dummy pattern 22a as a mask, for example, P, As, or B and BF2 are poured in by injection rate 1E13-1E14/cm2, and 1st impurity diffused layer 12a is formed.

[0050] Next, as shown in drawing 6 (a), after forming silicon oxide or 50nm of silicon nitrides etc. with a CVD method, 1st sidewall 13a is formed by the etchback method. Then, P, As, or B and BF2 are poured in by injection rate 1E15-1E16/cm2 with ion-implantation, and 2nd impurity diffused layer 14a is formed.

[0051] Next, as shown in drawing 6 (b), with a CVD method etc., 500-1000nm of insulator layers, for example, silicon oxide etc., is formed with a CVD method etc., flattening is carried out by the grinding method or the etchback method, and the pad insulator layer 28 is formed on the semi-conductor substrate 1 between the both sides of 1st dummy pattern 22a, and the 1st insulator layer 5.

[0052] Next, as shown in drawing 6 (c), after forming 2nd dummy pattern 22b, the 3rd impurity diffused layer 12a, the 2nd sidewall 13b, and 4th impurity diffused layer 14b in other fields by repeating the same process as drawing 5 (a) - drawing 6 (b), the pad insulator layer 28 is formed.

[0053] Next, as shown in drawing 6 (d), a resist pattern 23 is formed, the formation field of 2nd dummy pattern 22b is covered, and etching removal of the 1st mask film 2 which is in the lower part of 1st dummy pattern 22a with 1st dummy pattern 22a is carried out.

[0054] Next, as shown in drawing 7 (a), after removing a resist pattern 23, the 1st gate dielectric film 30 of desired thickness is formed in silicon oxide, a silicon nitride, a nitriding oxide film, a metal oxide film, metal nitriding oxide films, or these cascade screens on the semi-conductor substrate 1 of the part which removed dummy pattern (which shows example formed with CVD method in drawing) 22a with the oxidizing [thermally] method or the CVD method. Then, the doped polysilicon

film, a metal membrane, and a metal nitride are formed as 1st conductive film 15 with a CVD method etc.

[0055] Next, as shown in drawing 7 (b), flattening of the 1st conductive film 15 is carried out by the grinding method or the etchback method, and 1st gate electrode 29a is formed. Next, as shown in drawing 7 (c), the 2nd gate dielectric film 31 and 2nd gate electrode 29b are formed through the same process as drawing 6 (d) - drawing 7 (b). Similarly, the transistor which has a desired property in two or more fields can be formed.

[0056] Then, a wiring layer 20 is formed on a gate electrode through the same process as the gestalt 1 of the above-mentioned implementation. Since gate dielectric film is formed after formation of an impurity diffused layer not to mention doing so the same effectiveness as the gestalt 1 of the above-mentioned implementation, the semiconductor device of the gestalt 2 of the operation constituted as mentioned above can adopt a scarce ingredient as thermal resistance as gate dielectric film, for example among silicon oxide, a silicon nitride, a nitriding oxide film, a metal oxide film, metal nitriding oxide films, or these cascade screens, and can extend technical alternative.

[0057] Although how to change the thickness of gate dielectric film as an approach of controlling the threshold of a transistor by the gestalten 1 and 2 of the gestalt 3. above-mentioned implementation of operation was explained, how to change a gate electrode material as an approach of controlling the threshold of a transistor here is explained based on the gestalt 2 of the above-mentioned implementation. In addition, it cannot be overemphasized that the gestalt 1 of the above-mentioned implementation can be formed similarly.

[0058] Drawing 8 is the process sectional view showing the manufacture approach of the semiconductor device of the gestalt 3 implementation this invention. Sequential explanation is given according to drawing. First, as the 1st gate dielectric film 30 and 1st gate electrode 39a are formed, next it is shown in drawing 8 (a) like drawing 7 (b) through the same process as the gestalt 2 of the above-mentioned implementation, 2nd dummy pattern 22b is removed. Next, as shown in drawing 8 (b), the 2nd gate dielectric film 31 is formed with the oxidizing [thermally] method or a CVD method. Then, the 2nd conductive film 36 is formed in the whole surface with a CVD method etc. Next, as shown in drawing 8 (c), flattening of the 2nd conductive film 36 is carried out by the grinding method or the etchback method, and 2nd gate electrode 39b is formed.

[0059] At this time, 2nd gate electrode 39b forms the quality of the material by the side of gate dielectric film at least by different matter from the quality of the material which forms 1st gate electrode 39a. For example, when the quality of the material of 1st gate electrode 39a is polish recon, the quality of the material of 2nd gate electrode 39b is formed by the titanium nitride.

[0060] the quality of the material of this 1st and 2nd gate electrode 39a and 39b -- the ingredient of conductive film, such as polish recon, an amorphous silicon, silicide, a metal, a metal nitride, and a metal oxide film, and the cascade screen more than two-layer [these] -- it forms using the ingredient with which it differs [inner]. Furthermore, even if it is the same ingredient, a different work function by doping impurities, such as B, As, and P, may be realized.

[0061] According to the semiconductor device of the gestalt 3 of the operation constituted as mentioned above, in two transistors, even if it does not change the thickness of gate dielectric film, the threshold of each transistor is controllable by forming a gate electrode using the quality of the material from which a work function differs. Furthermore, a gate electrode material is easily changeable from the ability of a gate electrode to be independently formed in a desired field respectively with a desired ingredient.

[0062] Therefore, in the N type of a CMOS device, and a P type transistor, although it is effective especially when changing a gate electrode material, a still various functions device is realizable also with the transistor of the same mold by using a gate electrode material properly.

[0063] Moreover, also when the ingredient of the conductive film which contains metals, such as silicide, a metal, and a metal nitride, as a gate electrode especially is used, and an electrical

potential difference is impressed to a gate electrode, a depletion layer cannot be formed and the threshold shift accompanying increase of the effectual thickness of gate dielectric film can be prevented.

[0064] Although the gestalten 1 and 2 of the gestalt 4. above-mentioned implementation of operation explained the case where a gate electrode and a wiring layer were formed at another process, the case where a gate electrode and a wiring layer are formed in coincidence here is explained.

[0065] Drawing 9 is the process sectional view showing the manufacture approach of the semiconductor device of the gestalt 4 implementation this invention. Sequential explanation is given according to drawing. First, after forming as are shown in drawing 9 (a), and shown in drawing 4 (a) through the same process as the gestalt 1 of the above-mentioned implementation, 1st gate electrode 9a and 2nd gate electrode 9b are removed. Next, as shown in drawing 9 (b), for example, polish recon, an amorphous silicon, silicide, a metal, a metal nitride, a metal oxide film, about 200-1000nm of cascade screens more than two-layer [these] etc., etc. are formed in the whole surface as conductive film 25.

[0066] Next, as shown in drawing 9 (c), a resist pattern 24 is formed with a photo-engraving process. Next, as shown in drawing 9 (d), the conductive film 25 is etched by using a resist pattern 24 as a mask, and a gate electrode and a wiring layer are formed in one.

[0067] In one process, the semiconductor device of the gestalt 4 of the operation constituted as mentioned above can form two or more gate electrodes and wiring layers of a field at once, and can reduce a routing counter. Moreover, if the width of face of a resist pattern 24 is set up more widely than channel length, the increment in resistance of the wiring layer accompanying detailed-izing of a transistor can be prevented.

[0068] Gestalt 5. drawing 10 -12 of operation are the process sectional view showing the manufacture approach of the semiconductor device of the gestalt 5 implementation this invention. Sequential explanation is given according to drawing. First, as shown in drawing 10 (a), 10nm of silicon oxide is formed as 1st mask film 52 with the oxidizing [thermally] method or a CVD method on the semi-conductor substrate 51. Next, 150nm for example, of silicon nitrides is formed as 2nd mask film 53 with a CVD method. Then, a desired resist pattern (with no illustration) is formed by photoengraving process, and a trench 54 is formed in the semi-conductor substrate 1 by the etching method.

[0069] Next, as shown in drawing 10 (b), after forming silicon oxide in the whole surface as the 1st insulator layer 55 with a CVD method, the 1st insulator layer 55 on the 2nd mask film 53 is removed carrying out flattening by the grinding method, and the 1st insulator layer 55 is embedded in a trench 54.

[0070] Next, as shown in drawing 10 (c), after reducing the thickness of the 1st insulator layer 55 in a trench 54 by the wet etching methods, such as fluoric acid, the 2nd mask film 53 is alternatively removed by the wet etching methods, such as a heat phosphoric acid. Then, the 1st mask film 52 is further removed by the wet etching method.

[0071] Next, as shown in drawing 10 (d), about 2nm of silicon oxide is formed as 1st dummy film 56 by the oxidizing [thermally] method. Then, 200nm of 2nd dummy film 57 for dummy gate electrodes is formed in the whole surface, for example. Next, as shown in drawing 11 (a), a resist pattern 58 is formed by photoengraving process, and 1st dummy gate electrode 57a and 2nd dummy gate electrode 57b are formed by the etching method.

[0072] Next, as shown in drawing 11 (b), after removing a resist pattern 58, P, As, or B and BF2 are poured in by injection rate 1E13-1E14/cm2 with ion-implantation, and the 1st impurity diffused layer 61a and 61b is formed. Furthermore, after forming silicon oxide or 50nm of silicon nitrides etc. with a CVD method, Sidewalls 60a and 60b are formed by the etchback method. Then, P, As, or B and BF2 are poured in by injection rate 1E15-1E16/cm2 with ion-implantation, and the 2nd impurity diffused layer 59a and 59b is formed.

[0073] Next, as shown in drawing 11 (c), 500nm of insulator layers 62, such as silicon oxide, is formed in the whole surface with a CVD method etc. Next, flattening of the insulator layer 62 is carried out until the front face of the dummy gate electrodes 57a and 57b is exposed by the grinding method or the etchback method, as shown in drawing 11 (d).
[0074] Next, as shown in drawing 12 (a), a resist pattern 63 is formed, the formation field of 2nd dummy gate electrode 57b is covered, and etching removal of the 2nd dummy film 56 of 1st dummy gate electrode 57a and the 1st dummy gate electrode 57a lower part is carried out. Next, as shown in drawing 12 (b), after removing a resist pattern 63, the 1st gate dielectric film 64 of desired thickness is formed for silicon oxide, a silicon nitride, a nitriding oxide film, a metal oxide film, metal nitriding oxide films, or these cascade screens on the semi-conductor substrate 51 of the part which removed dummy gate electrode 57a with the oxidizing [thermally] method or a CVD method (the example formed with a CVD method in drawing is shown). Then, the doped polysilicon film, a metal membrane, and a metal nitride are formed as 1st conductive film 65 with a CVD method etc.
[0075] Next, as shown in drawing 12 (c), flattening of the 1st conductive film 65 is carried out by the grinding method or the etchback method, and 1st gate electrode 65a is formed. Then, although illustration is omitted, by repeating the process shown in drawing 12 (a), (b), and (c) to the field of other requests, the transistor which changed the thickness of gate dielectric film is formed in a different field, and wiring is formed by giving photoengraving process and the etching method to the conductive film.
[0076] Since the semiconductor device of the gestalt 5 of the operation constituted as mentioned above can form a transistor in two or more fields independently, it can form independently desired gate dielectric film and a desired gate electrode separately. Furthermore, since gate dielectric film is formed after formation of an impurity diffused layer, a scarce ingredient can also be used for thermal resistance as gate dielectric film, and the degree of freedom of selection of a gate-dielectric-film ingredient spreads.
[0077]
[Effect of the Invention] Two or more 1st insulator layers which were embedded as mentioned above in two or more slots formed in the semi-conductor substrate according to claim 1 of this invention, Two or more gate dielectric film formed on the above-mentioned semi-conductor substrate between the insulator layers of the above 1st, Two or more gate electrodes formed on two or more above-mentioned gate dielectric film, respectively, The impurity diffused layer formed into the above-mentioned semi-conductor substrate of two or more above-mentioned gate electrode both sides, Since it was made to have the property that the transistors which are equipped with the 2nd insulator layer embedded two or more above-mentioned gate inter-electrode, and consist of gate dielectric film, a gate electrode, and an impurity diffused layer differ for two or more fields of every For every transistor from which a property differs, desired gate dielectric film and a desired gate electrode can be formed, and a good multifunctional device is obtained independently.
[0078] Moreover, according to claim 2 of this invention, since it was made, as for the transistor of a different property, for the thickness of gate dielectric film to have thickness different, respectively mutually, a multifunctional device is certainly obtained with a sufficient precision.
[0079] Moreover, according to claim 3 of this invention, since it was made for the quality of the material of a gate electrode to consist of the quality of the material different, respectively mutually, the transistor of a different property can control the threshold of a transistor by the work function of each gate electrode quality-of-the-material proper, and a various functions device can realize it with a sufficient precision certainly.
[0080] Moreover, since it was made for the quality of the material of a gate electrode to be the conductive film containing a metal according to claim 4 of this invention, also when an electrical potential difference is impressed to a gate electrode, a depletion layer cannot be formed and effectual increase of the thickness of gate dielectric film can be prevented.

[0081] Furthermore, the manufacture approach of the semiconductor device of claim 5 this invention The 1st process which forms the mask film on a semi-conductor substrate, and the 2nd process which carries out patterning of the above-mentioned mask film and the above-mentioned semi-conductor substrate, and forms a slot, The 3rd process which embeds a separation insulator layer at above-mentioned Mizouchi, and the 4th process which removes the above-mentioned mask film of the field of the request of two or more above-mentioned fields, The 5th process which forms desired gate dielectric film on the above-mentioned semi-conductor substrate of the field of the above-mentioned request, Since it was made to have with the 7th process which performs repeatedly the 6th process which forms the desired conductive film on the above-mentioned gate dielectric film, and the 4th process of the above, the 5th process and the 6th process to the field of other requests one by one While being able to form a transistor in two or more different fields independently, being able to form desired gate dielectric film independently separately and being able to form the gate dielectric film with which thickness differs good The 1st insulator layer is projected and formed on the semi-conductor substrate, retreats from a semi-conductor substrate front face, and does not form a crevice. Therefore, metal-oxide-semiconductor structure is formed in the side attachment wall of a crevice, unnecessary electric field are generated, and it can prevent degrading the property of a transistor.

[0082] Moreover, according to claim 6 of this invention, since it was made to perform a resist pattern as a mask and a resist pattern does not contact gate dielectric film directly, resist ****** does not occur on gate dielectric film, and film decrease of gate dielectric film does not produce the 4th process of claim 5 in the washing process after a resist removal process.

[0083] Moreover, the 8th process which according to claim 7 of this invention carries out patterning of the conductive film of the field of the request of two or more fields, and forms a gate electrode after the 7th process according to claim 5, The 9th process which forms an impurity diffused layer in the semi-conductor substrate of the both sides of the above-mentioned gate electrode, Since it had the process which performs repeatedly the 10th process which embeds on the semi-conductor substrate between the both sides of the above-mentioned gate electrode, and a separation insulator layer, and forms an insulator layer, and the 8th process, the 9th process and the 10th process to the field of other requests one by one A transistor can be formed in two or more different fields independently, and a desired gate electrode can be separately formed independently.

[0084] Moreover, the 1st process which forms the mask film on a semi-conductor substrate according to claim 8 of this invention, The 2nd process which carries out patterning of the above-mentioned mask film and the above-mentioned semi-conductor substrate, and forms a slot, The 3rd process which embeds a separation insulator layer at above-mentioned Mizouchi, and the 4th process which carries out patterning of the above-mentioned mask film, and forms a dummy pattern, The 5th process which forms an impurity diffused layer in the above-mentioned semi-conductor substrate of the both sides of the above-mentioned dummy pattern, The 6th process which forms an insulator layer on the above-mentioned semi-conductor substrate between the both sides of the above-mentioned dummy pattern, and the above-mentioned separation insulator layer, The 8th process which removes the above-mentioned dummy pattern of the field of the request of two or more above-mentioned fields, The 9th process which forms desired gate dielectric film on the above-mentioned semi-conductor substrate of the above-mentioned dummy pattern removal field, Since it had the 11th process which performs repeatedly the 10th process which forms a desired gate electrode on the above-mentioned gate dielectric film, and the 8th process of the above, the 9th process and the 10th process to the field of a request of others [above] one by one A transistor can be formed in two or more different fields independently, desired gate dielectric film can be separately formed independently, and the gate dielectric film with which thickness differs can be formed good. Furthermore, a scarce ingredient can also be used for thermal resistance as gate dielectric film, and the degree of freedom of selection of a gate-dielectric-film ingredient spreads.

[0085] Moreover, the 1st process which according to claim 9 of this invention carries out patterning

of the semi-conductor substrate, and forms a slot, The 2nd process which carries out flattening of the above-mentioned semi-conductor substrate front face by embedding a separation insulator layer at above-mentioned Mizouchi, The 3rd process which forms the 1st dummy film and the 2nd dummy film in the whole surface in order, The 4th process which carries out patterning of the dummy film of the above 2nd, and forms two or more dummy gate electrodes, The 5th process which forms an impurity diffused layer in the above-mentioned semi-conductor substrate of the both sides of two or more above-mentioned dummy gate electrodes, The 6th process which forms an insulator layer so that two or more above-mentioned dummy gate electrodes may be covered, The 7th process which carries out flattening until the above-mentioned dummy gate electrode exposes the above-mentioned insulator layer, The 8th process which removes the above-mentioned dummy gate electrode and dummy gate dielectric film of a field of the request of two or more above-mentioned fields, The 9th process which forms desired gate dielectric film on the above-mentioned semi-conductor substrate of the above-mentioned dummy gate electrotreatment field, Since it had the 11th process which performs repeatedly the 10th process which forms a desired gate electrode on the above-mentioned gate dielectric film, and the 8th process of the above, the 9th process and the 10th process to the field of a request of others [above] one by one Since a transistor can be formed in two or more fields independently, desired gate dielectric film and a desired gate electrode can be separately formed independently. Furthermore, since gate dielectric film is formed after formation of an impurity diffused layer, a scarce ingredient can also be used for thermal resistance as gate dielectric film, and the degree of freedom of selection of a gate-dielectric-film ingredient spreads.

[0086] Moreover, since the transistor from which a property differs by forming for every field so that the thickness of gate dielectric film may differ, respectively was formed according to claim 10 of this invention, the transistor which has a different property can be formed with the yield sufficient good in the same LSI, and a various functions device can be formed easily.

[0087] Moreover, since the transistor from which a property differs by forming for every field so that the ingredients of a gate electrode may differ, respectively was formed according to claim 11 of this invention, the transistor which has a different property can be formed with the yield sufficient good in the same LSI, and even if the thickness of gate dielectric film is fixed, a various functions device can be formed easily.

[0088] Moreover, since the wiring layer was formed on the gate electrode according to claim 12 of this invention, if the width of face of a wiring layer is set up more widely than channel length, the increment in resistance of the wiring layer accompanying detailed-izing of a transistor can be prevented.

[0089] According to claim 13 of this invention, moreover, the process which forms a wiring layer on a gate electrode Since it was made to be the process which removes the above-mentioned gate electrode, the process which forms the conductive film in the whole surface, and the process which carries out patterning of the above-mentioned conductive film, and unified and forms the above-mentioned wiring layer and the above-mentioned gate electrode In one process, two or more gate electrodes and wiring layers of a field can be formed at once, and a routing counter can be reduced.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original

precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the process sectional view showing the manufacture approach of the semiconductor device of the gestalt 1 implementation this invention.
[Drawing 2] It is the process sectional view showing the manufacture approach of the semiconductor device of the gestalt 1 implementation this invention.
[Drawing 3] It is the process sectional view showing the manufacture approach of the semiconductor device of the gestalt 1 implementation this invention.
[Drawing 4] It is the process sectional view showing the manufacture approach of the semiconductor device of the gestalt 1 implementation this invention.
[Drawing 5] It is the process sectional view showing the manufacture approach of the semiconductor device of the gestalt 2 implementation this invention.
[Drawing 6] It is the process sectional view showing the manufacture approach of the semiconductor device of the gestalt 2 implementation this invention.
[Drawing 7] It is the process sectional view showing the manufacture approach of the semiconductor device of the gestalt 2 implementation this invention.
[Drawing 8] It is the process sectional view showing the manufacture approach of the semiconductor device of the gestalt 3 implementation this invention.
[Drawing 9] It is the process sectional view showing the manufacture approach of the semiconductor device of the gestalt 4 implementation this invention.
[Drawing 10] It is the process sectional view showing the manufacture approach of the semiconductor device of the gestalt 5 implementation this invention.
[Drawing 11] It is the process sectional view showing the manufacture approach of the semiconductor device of the gestalt 5 implementation this invention.
[Drawing 12] It is the process sectional view showing the manufacture approach of the semiconductor device of the gestalt 5 implementation this invention.
[Drawing 13] It is the process sectional view showing the manufacture approach of the conventional semiconductor device.
[Drawing 14] It is the process sectional view showing the manufacture approach of the conventional semiconductor device.
[Description of Notations]
1 51 2 A semi-conductor substrate, 52 3 The 1st mask film, 53 2nd mask film, 4 54 5 A trench, 55 The 1st insulator layer, 9a, 19a, 29a, 39a, 65a The 1st gate electrode, 9b, 19b, 29b, 39b The 2nd gate electrode, 10, 30, 64 The 1st gate dielectric film, 11 31 The 2nd gate dielectric film, 12a, 61a, 61b The 1st impurity diffused layer, 12b The 3rd impurity diffused layer, 14a, 59a, 59b The 2nd impurity diffused layer, 14b The 4th impurity diffused layer, 15 16 The 1st conductive film and 36 2nd conductive film, 25 The conductive film, 20 A wiring layer, 22a The 1st dummy pattern, 22b 23 The 2nd dummy pattern, 70 A resist pattern, 56 The 1st dummy film, 57 The 2nd dummy film, 57a The 1st dummy gate electrode, 57b 2nd dummy gate electrode.

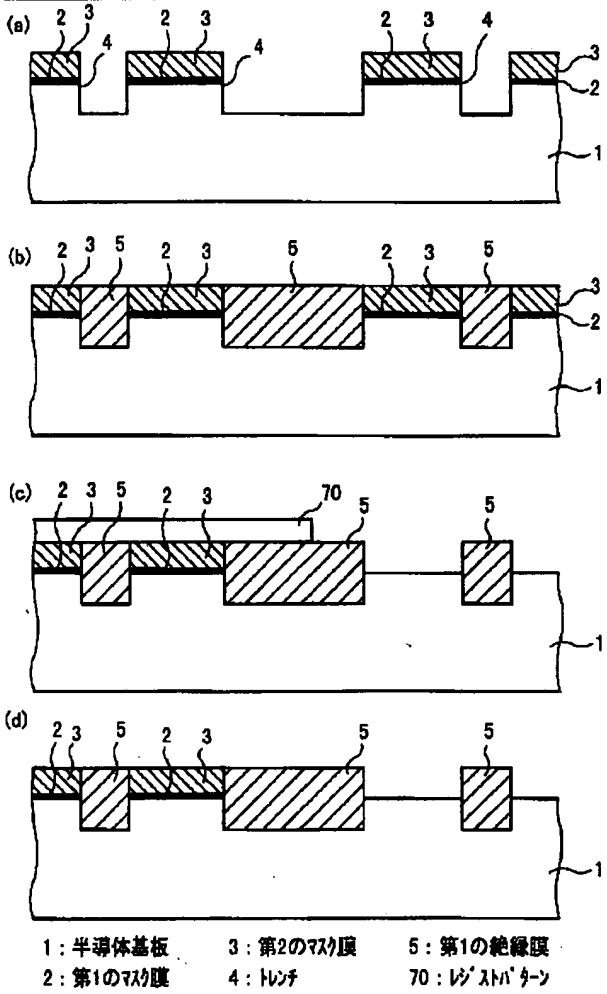
[Translation done.]

* NOTICES *

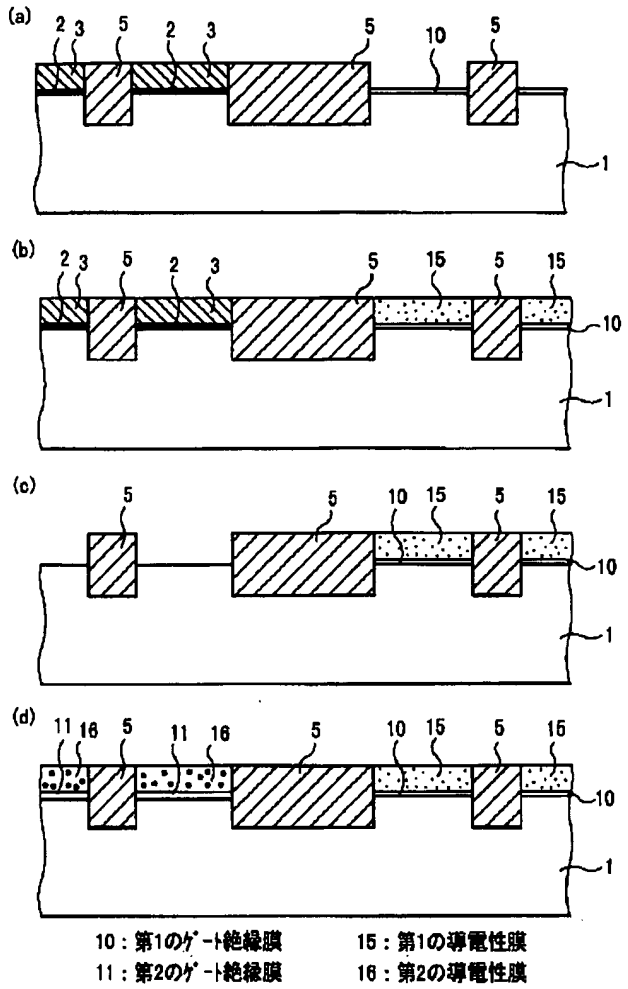
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

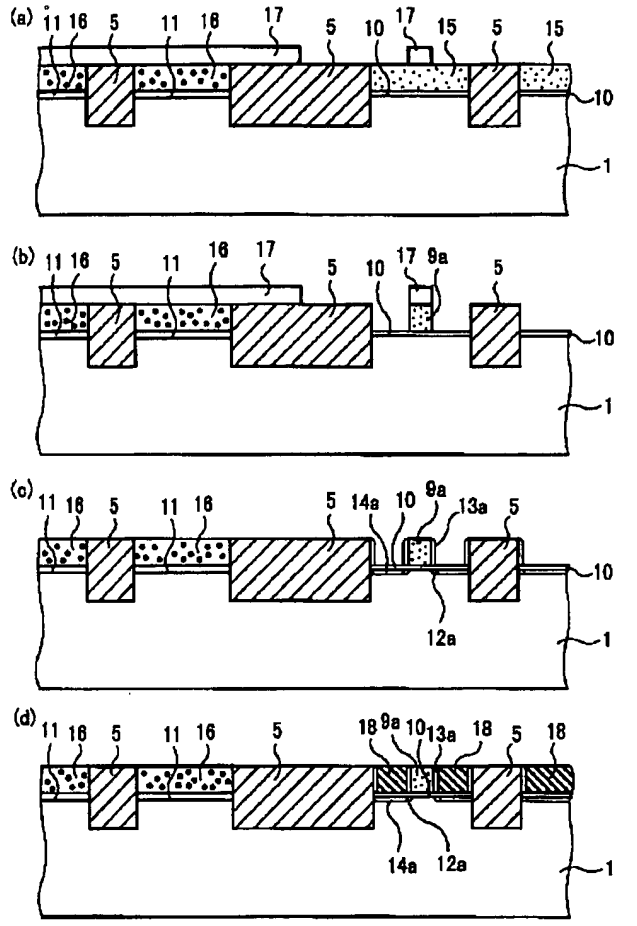
[Drawing 1]



[Drawing 2]

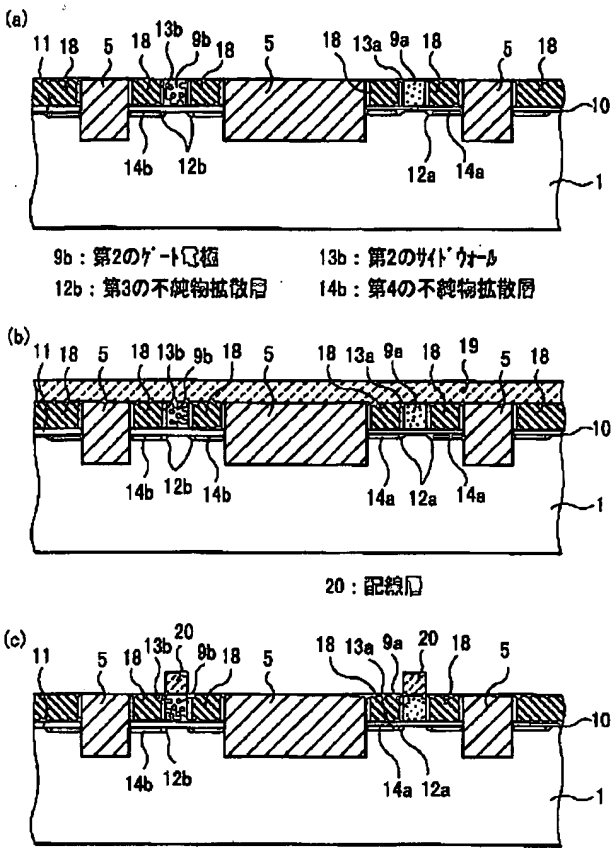

(a)
2 3 5 2 3 5 10 5
1
(b)
2 3 5 2 3 5 15 5 15
10
1
(c)
5 5 10 15 5 15
10
1
(d)
11 16 5 11 16 5 10 15 5 16
10
1
10：第1のｹﾞｰﾄ絶縁膜
11：第2のｹﾞｰﾄ絶縁膜
15：第1の導電性膜
16：第2の導電性膜

[Drawing 3]

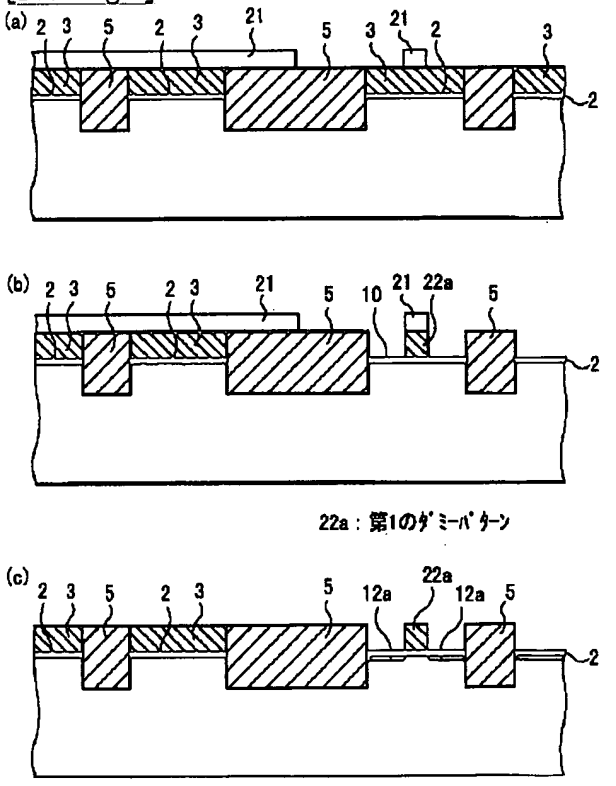


9a：第1のｹﾞｰﾄ電極　13a：第1のｻｲﾄﾞｳｫｰﾙ　18：埋込み絶縁膜
12a：第1の不純物拡散層　14a：第2の不純物拡散層

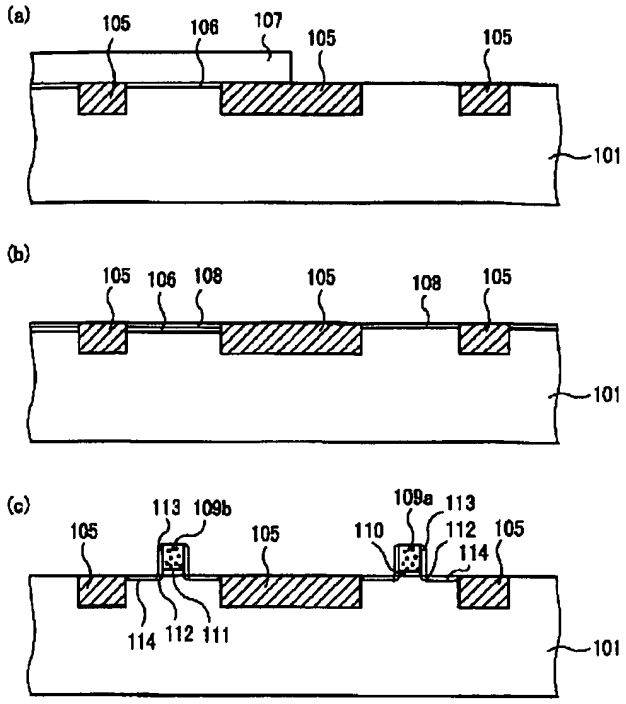
[Drawing 4]



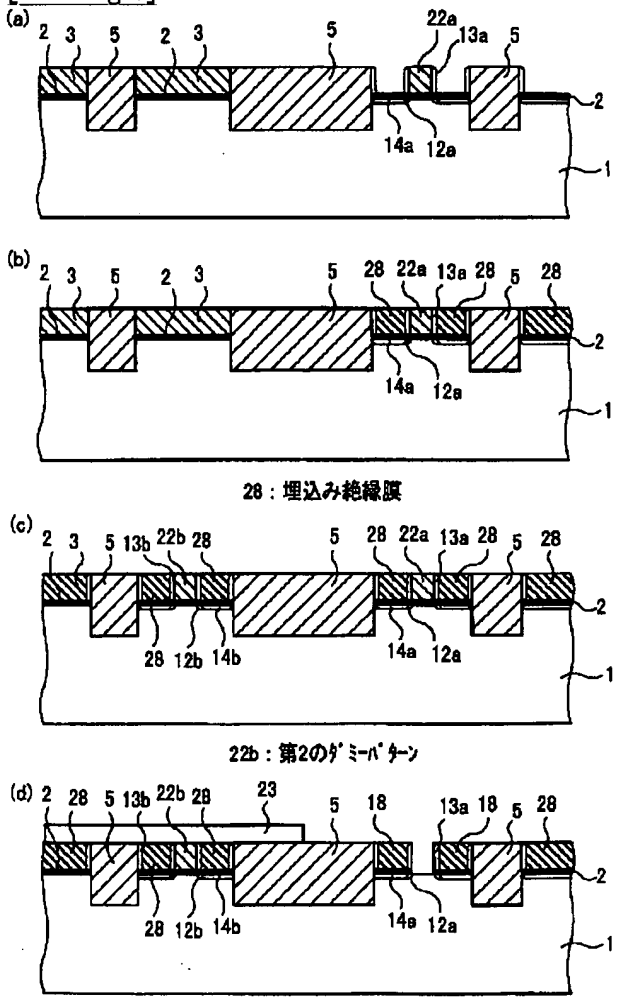
[Drawing 5]



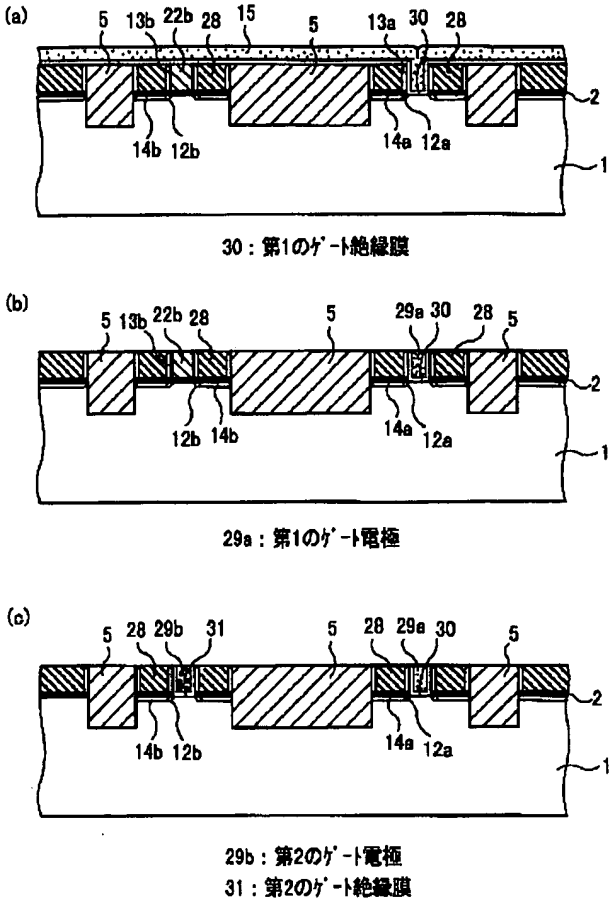
[Drawing 14]



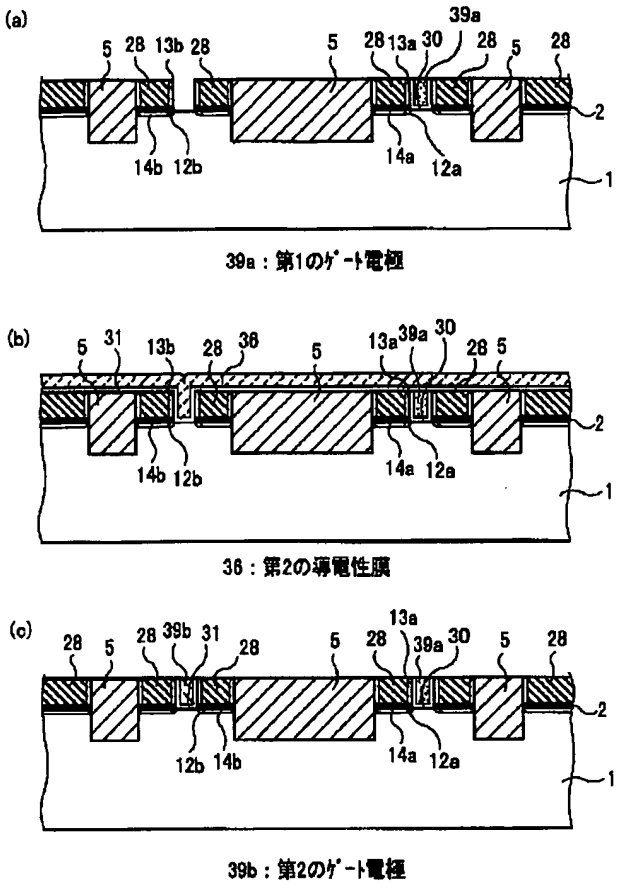
[Drawing 6]



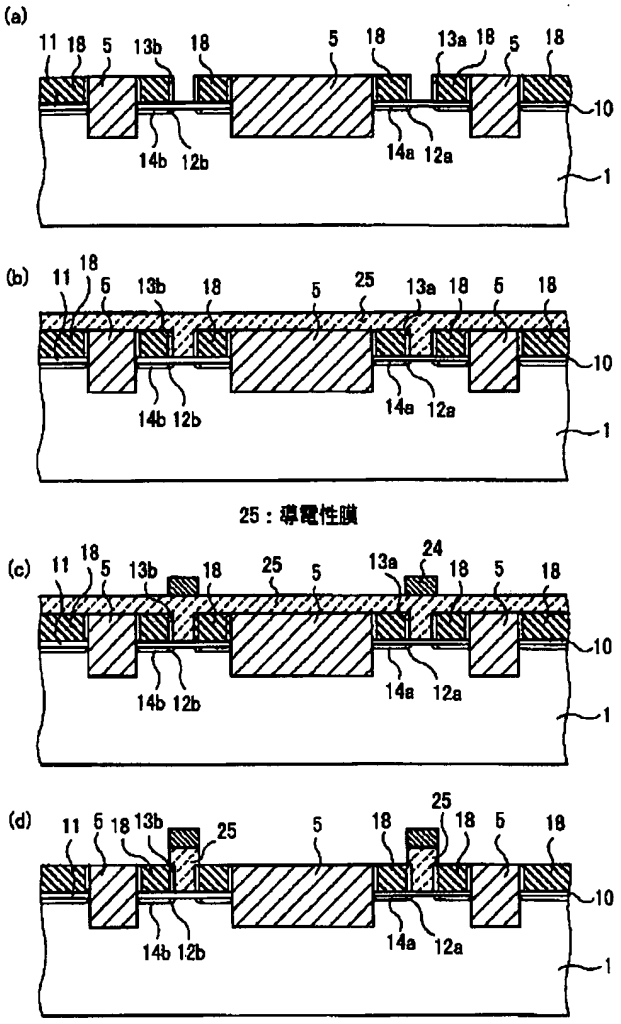
[Drawing 7]


(a)
5 13b 22b 28 15 5 13a 30 28
2
14b 12b 14a 12a
1
30：第1のｹﾞｰﾄ絶縁膜
(b)
5 13b 22b 28 5 29a 30 28 5
2
12b 14b 14a 12a
1
29a：第1のｹﾞｰﾄ電極
(c)
5 28 29b 31 5 28 29a 30 5
2
14b 12b 14a 12a
1
29b：第2のｹﾞｰﾄ電極
31：第2のｹﾞｰﾄ絶縁膜

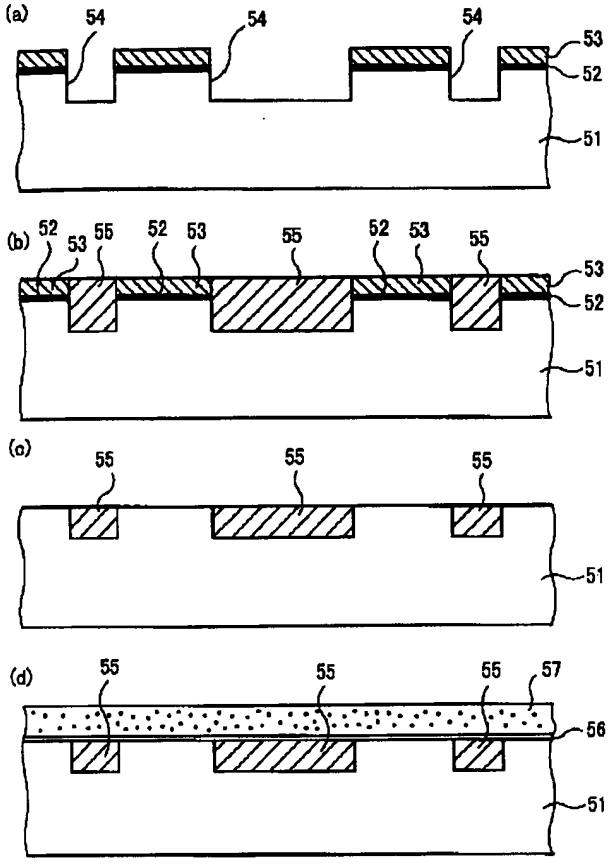
[Drawing 8]


(a)
39a
5 28 13b 28 5 28 13a 30 28 5 28
2
14b 12b 14a 12a
1
39a：第1のｹﾞｰﾄ電極
(b)
5 31 13b 28 38 5 13a 39a 30 28 5
2
14b 12b 14a 12a
1
38：第2の導電性膜
(c)
13a
28 5 28 39b 31 28 5 28 39a 30 5 28
2
12b 14b 14a 12a
1
39b：第2のｹﾞｰﾄ電極

[Drawing 9]

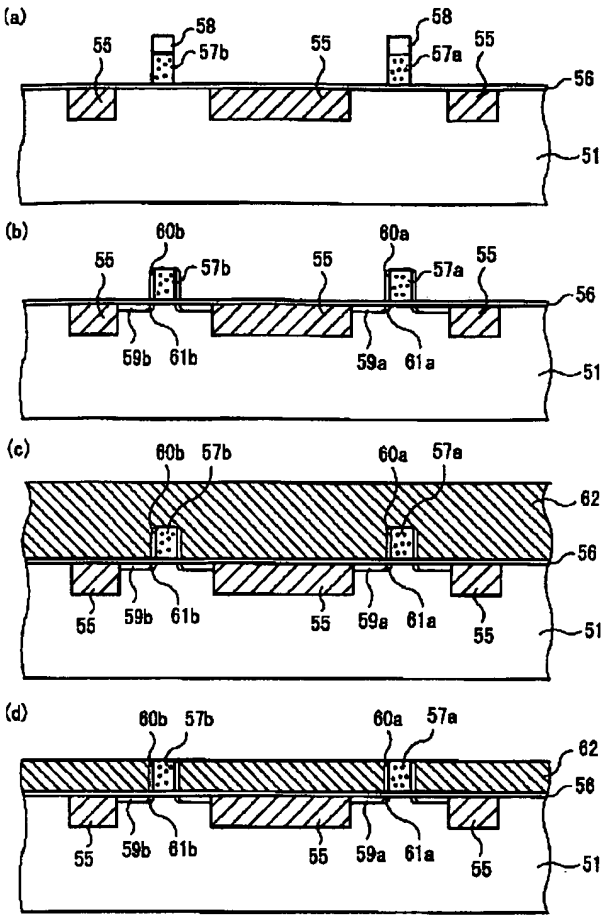

(a)
11 18 5 13b 18 5 18 13a 18 5 18
10
14b 12b 14a 12a
1
(b)
11 18 6 13b 18 5 25 13a 18 6 18
10
14b 12b 14a 12a
1
25：導電性膜
(c)
11 18 5 13b 18 25 5 13a 24 18 5 18
10
14b 12b 14a 12a
1
(d)
11 5 18 13b 25 5 18 25 18 5 18
10
14b 12b 14a 12a
1

[Drawing 10]



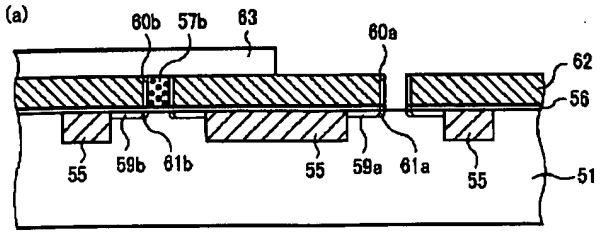
51：半導体基板　54：トレンチ　56：第1のダミー膜
52：第1のマスク膜　55：第1の絶縁膜　57：第2のダミー膜
53：第2のマスク膜

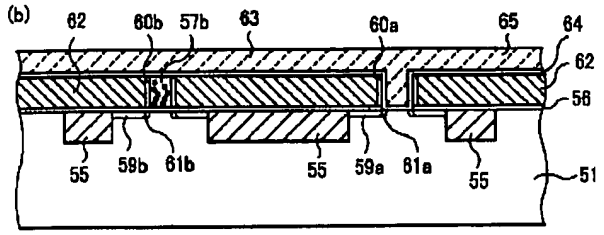
[Drawing 11]



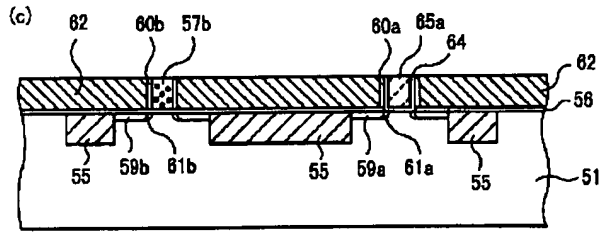
57a : 第1のゲート電極
57b : 第2のゲート電極
59a, 59b : 第2の不純物拡散層
61a, 61b : 第1の不純物拡散層
62 : 絶縁膜

[Drawing 12]



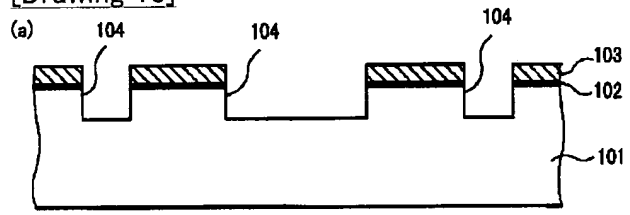


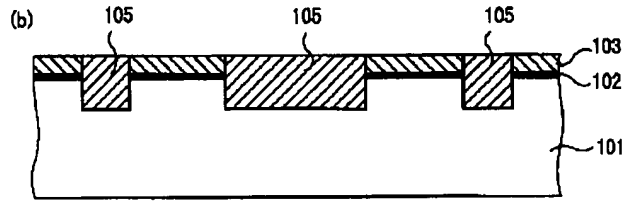
64：第1のｹﾞｰﾄ絶縁膜

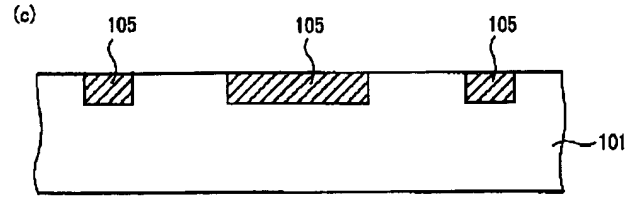


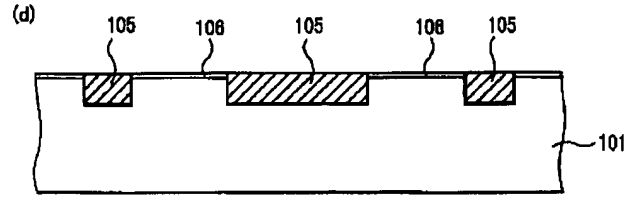
65a：第1のｹﾞｰﾄ電極

[Drawing 13]









[Translation done.]